along with exemplary EDPs. The end of the leading cycle as illustrated includes time stamps 186 through 191 while the beginning of the following cycle includes time stamps 0 through 5. The EDPs that have time stamps during the leading cycle are identified by downwardly directed arrows while the EDPs that have time stamps during the following cycle are identified by upwardly directed arrows. Six exemplary EDPs 1l, 2l, 3l, 4l, 5l and 6l are illustrated with EDPs 1l, 2l and 3l occurring during the leading clock cycle and having time stamps 186, 188 and 190, respectively, while EDPs 4l, 5l and 6l occur during the following clock cycle and having time stamps 0, 2 and 5.

[0012] For this example, assume that the EDPs 1l, 2l, 3l, 4l, 5l and 6l correspond to three separate annihilation events. In addition, assume a coincidence window W period corresponding to 12 consecutive time stamps. In this case, half the coincidence window (i.e., W/2) corresponds to six time stamp periods and therefore, any two EDPs having time stamps within 6 time stamp periods of each other should be considered for coincidence pairing.

[0013] Thus, referring still to Fig. 4, while EDPs 1l, 2l, 3l, 4l, 5l and 6l correspond to three separate annihilation events, potential coincidence pairs may include EDPs 1l and 2l (i.e., EDPs 1l and 2l may correspond to a single event), EDPs 2l and 3l, EDPs 3l and 4l, EDPs 4l and 5l, EDPs 5l and 6l, EDPs 1l and 3l, EDPs 1l and 4l, EDPs 2l and 4l, EDPs 2l and 5l, EDPs 3l and 4l, EDPs 3l and 5l and EDPs 4l and 6l. Nevertheless, exemplary coincidence detection circuitry would fail to recognize many of the potential coincidence pairings because the circuitry would not compare EDP time stamps between the leading and following cycles. Specifically, in this example, in the leading cycle, the coincidence circuitry would consider pairing EDPs 1l and 2l, 2l and 3l and 1l and 3l, while in the following cycle the circuitry would consider pairing EDPs 4l and 5l, 4l and 6l and 5l and 6l. The circuitry would ignore possible EDP pairings 2l and 4l, 2l and 5l, 3l and 4l, and 3l and 5l. Thus, assuming that, based on other signal characteristics (e.g., angles between crystals that generate EDPs, etc.), the coincidence circuitry identifies coincidence pairs including EDPs 1l and EDPs 2l and 5l and 6l ("found and accepted" pairs as illustrated), the

circuitry would miss the potential pair including EDPs 3l and 4l ("missed, no match" as illustrated).

[0037] Station 15 includes a CPU 50, a CRT display 51 and a keyboard 52. CPU 50 connects to network 18 and scans key board 52 for input information. Through the keyboard 52 and associated control panel switches, an operator can control calibration of system 9, its configuration, and the positioning of a patient table (not illustrated) ~~13~~ during data acquisition.

[0045] Referring still to Fig. 3, while circuitry 200 may include many additional components, for the purposes of this explanation, coincidence detection circuitry 200 includes a cycle extender 61, a time stamp duplicator 63, comparison circuitry 67 and a duplicate eliminator 69. Referring also to Fig. 5, a timing diagram 100 similar to diagram 98 in Fig. 4 illustrates operation of the coincidence detection components in accordance with the present invention and includes time stamps 186 through 197 that correspond to an extended first clock cycle and stamps 1 through 5 that correspond to a second clock cycle. Diagram 100 is different than diagram in 98 in several ways. First, consistent with the present invention, the diagram 100 includes an overlap period having a duration of W/2 (i.e., six times the time stamp period) that has been tacked onto the leading cycle. This extending process is facilitated by cycle extender 61. The resulting leading cycle is identified in Fig. 5 as an "extended leading cycle" with the overlap period, as the label implies, overlapping the following cycle by W/2.

[0046] Second, each of the time stamps corresponding to EDPs 4l, 5l and 6l in the following cycle that occur during the overlap period have been copied or duplicated in the overlap period. To this end, EDP 4l having a time stamp of 0 in the following cycle has been copied to time stamp 192 as EDP 4l' in the extended cycle, EDP 5l having a time stamp of 2 in the following cycle has been copied to time stamp 194 as EDP 5l' in the extended leading, EDP 6l having a time stamp of 5 in the following cycle has been copied to time stamp 197 as EDP 6l' in the extended leading cycle. This duplicating process is accomplished by duplicator 63.

[0047] After the EDP time stamps from the following cycle that occurs during the overlap period have been copied to the overlap period, comparison circuitry 67 compares all of the EDP time stamps in the extended leading cycle to identify coincidence pairs. Thus, in the present example, because each of EDPs 1l, 2l, 3l, 4l', 5l' and 6l' have time stamps that are in the extended leading cycle, each possible coincidence pair including time stamps corresponding to EDPs 1l and 2l, 2l and 3l, 3l and 4l', 4l' and 5l', 5l' and 6l', 1l and 3l, 1l and 4l', 2l and 4l', 2l and 5l', 3l and 4l', 3l and 5l' and 4l' and 6l' are considered for coincidence pairing. In the present case, as in the case of Fig. 4, the pair including EDPs 1l and 2l and the pair

including EDPs 5l' and 6l' are identified during extended period comparison. In addition, the pair including EDPs 3l and 4l' is also identified. The identified coincidence pairs are provided to duplicate eliminator 69.

[0048] After all of the coincidence pairs in the extended leading period have been identified, assembly 11 performs the same process with the following clock cycle as a new leading clock cycle and the clock cycle that comes after the following clock cycle as a new following clock cycle. Thus, referring again to Fig. 5, comparison circuitry 67 processes each of the EDPs having time stamps in the overlap period (i.e., following cycle EDPs having time stamps that occur during the extension period) a second time. In the present case this means that assembly 11 would process EDPs 4l, 5l and 6l despite the fact that copies 4l', 5l' and 6l' have already been processed once. Such dual processing would result in double counting of the coincidence pair including EDPs 5l and 6l and thus would cause a data acquisition error.

[0050] While the invention has been described above as one wherein clock cycles are extended by adding an extension period to the ends of the cycles, the present invention also contemplates embodiments where clock cycles are extended by adding an extension period to the beginning of each clock cycle. To this end, referring to Fig. 6, a diagram 102 illustrates the end of a leading and the beginning of a following clock cycle in a fashion similar to that in Fig. 5. In Fig. 6, however, an overlap period W/2 (i.e., again, the duration defined by 6 time stamps including stamps –6, -5, -4, -3, -2 and ~~through~~ -1) is added to the beginning of the following period instead of at the end of the leading period. In this case the time stamps corresponding to the EDPs in the overlap period (i.e., leading cycle EDPs having time stamps that occur during the overlap period) are copied to the extended following cycle and more specifically to the overlap period. Thus, EDP 1l having a time stamp of 186 in the leading cycle has been copied to time stamp -6 as EDP 1l' in the extended following cycle, EDP 2l having a time stamp of 188 in the leading cycle has been copied to time stamp -4 as EDP 2l' in the extended following cycle and EDP 3l having a time stamp of 190 in the leading cycle has been copied to time stamp -2 as EDP 3l' in the extended following cycle. Referring also to Fig. 3, the extending and copying processes are carried out by extender and duplicator 61 and 63, respectively in a manner similar to that described above.

[0054] Continuing, at block 156, duplicator 63 identifies overlap events that occur during the overlap period in the first of the master cycles. For example, referring again to Fig. 5, where the following cycle is the first cycle, duplicator 63 identifies EDPs 4l, 5l and 6l which each occur during the overlap period. Next, at block 158, duplicator 63 copies EDP time stamps (e.g., the EDPs) to the overlap period. Thus, as in Fig. 5, EDP stamps 4l, 5l and 6l are copied as stamps 4l', 5l' and 6l'.